Microprocessor with Branch Control Apparatus

FIG. 1

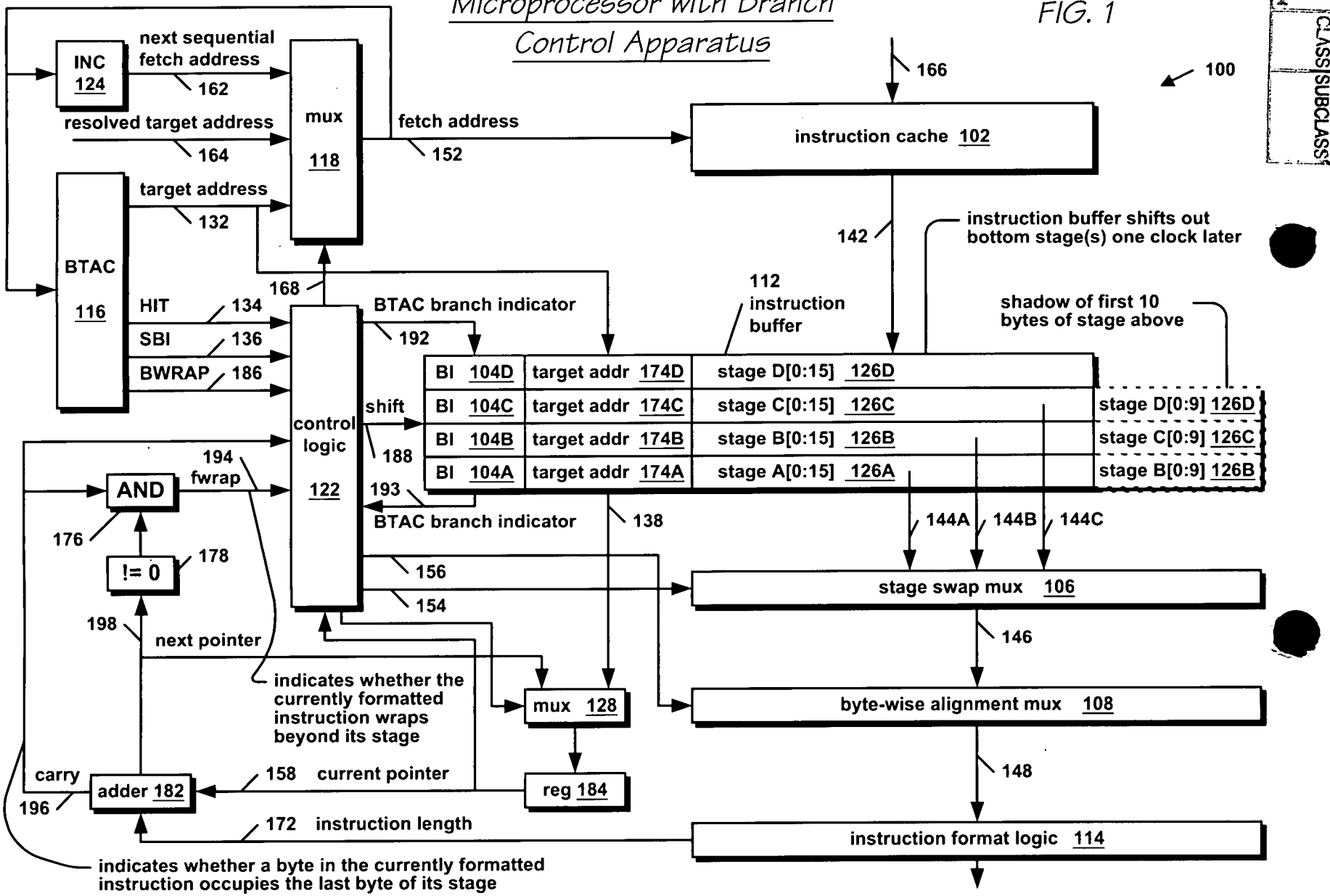
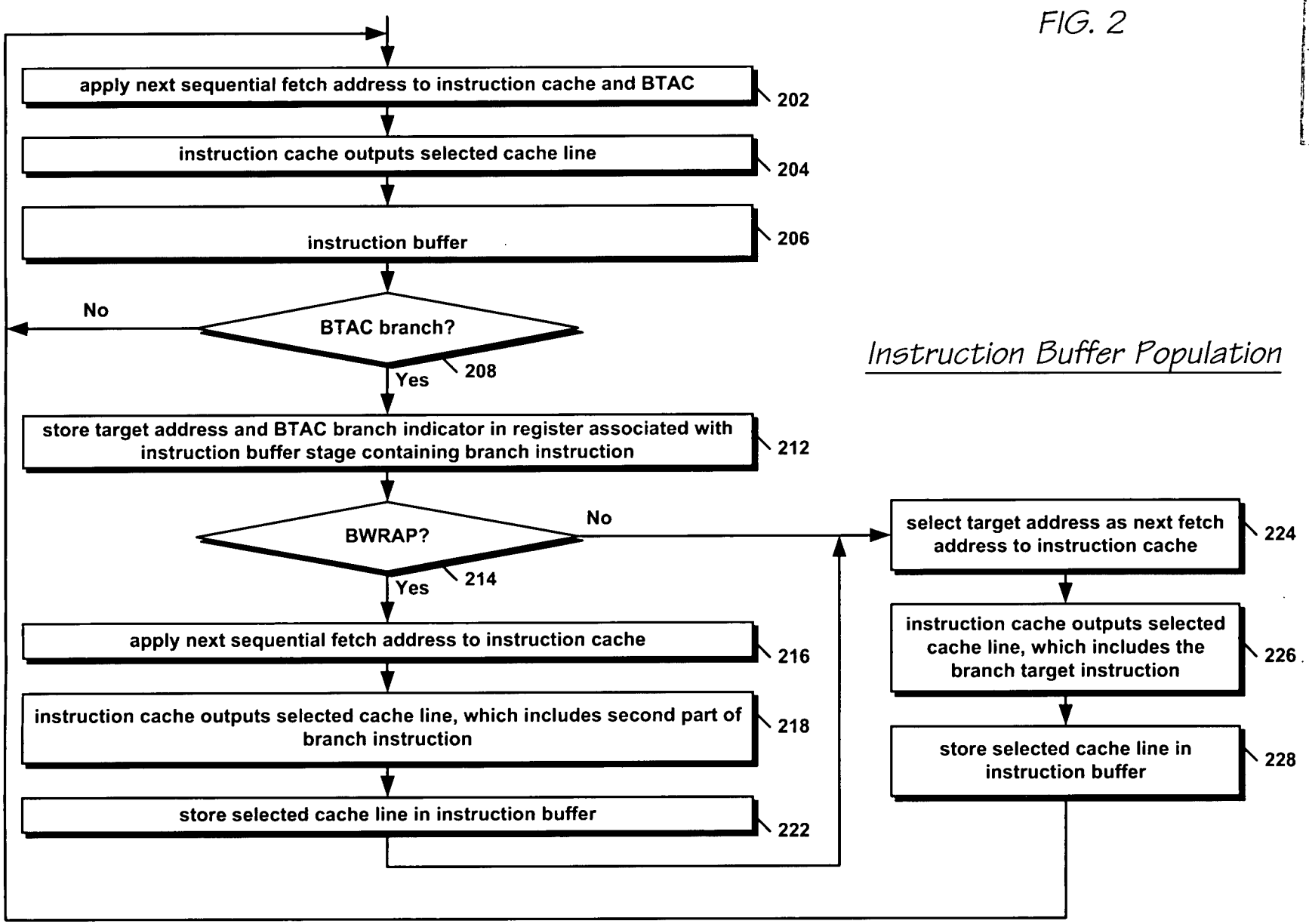
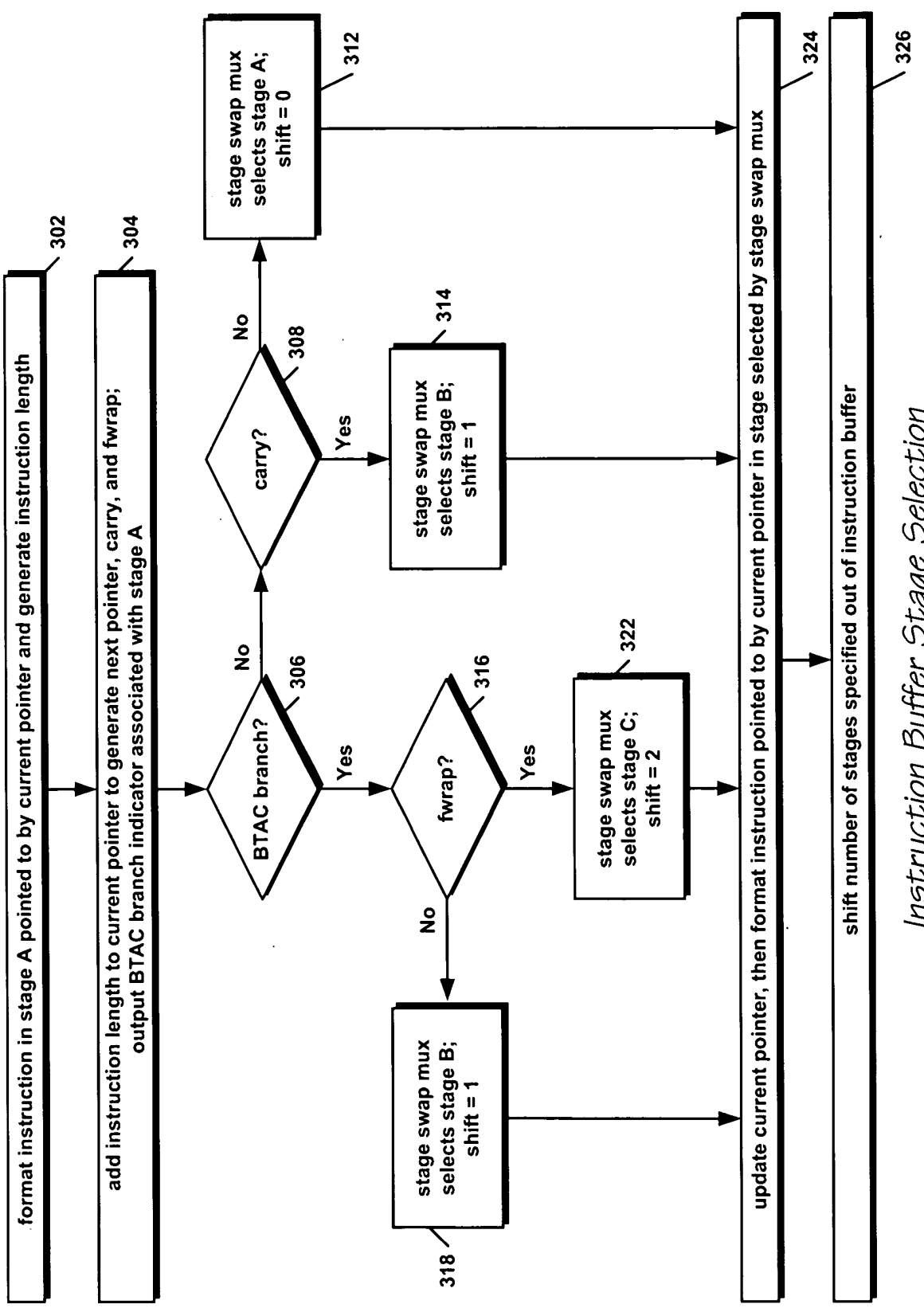


FIG. 2



Instruction Buffer Population

FIG. 3



Instruction Buffer Stage Selection

Figure 4A

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
																stage D
																stage C
																stage B
								ADD [0]	ADD [1]	ADD [2]	SUB [0]	SUB [1]	SUB [2]	SUB [3]		stage A

current pointer = 8
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 11
carry = false
fwrap = false

stage swap mux selects stage A

shift = 0

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Instruction Buffer Stage Selection Example: Case 1

Figure 4B

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
																stage D
																stage C
SUB [0]	SUB [1]	SUB [2]	SUB [3]													stage B
													ADD [0]	ADD [1]	ADD [2]	stage A

current pointer = 13
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 0
carry = true
fwrap = false

stage swap mux selects stage B

shift = 1

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Instruction Buffer Stage Selection Example: Case 2

Figure 4C

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
																stage D
																stage C
ADD [2]	SUB [0]	SUB [1]	SUB [2]	SUB [3]												stage B
														ADD [0]	ADD [1]	stage A

current pointer = 14
instruction length = 3
BTAC branch indicator = false
target address[0:3] = n/a

next pointer = 1
carry = true
fwrap = true

stage swap mux selects stage B

shift = 1

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Instruction Buffer Stage Selection Example: Case 3

Figure 4D

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
																stage D
																stage C
											SUB [0]	SUB [1]	SUB [2]	SUB [3]		stage B
							JCC [0]	JCC [1]								stage A

current pointer = 7
instruction length = 2
BTAC branch indicator[7] = true
target address[0:3] = 11

next pointer = 9
carry = false
fwrap = false

stage swap mux selects stage B

shift = 1

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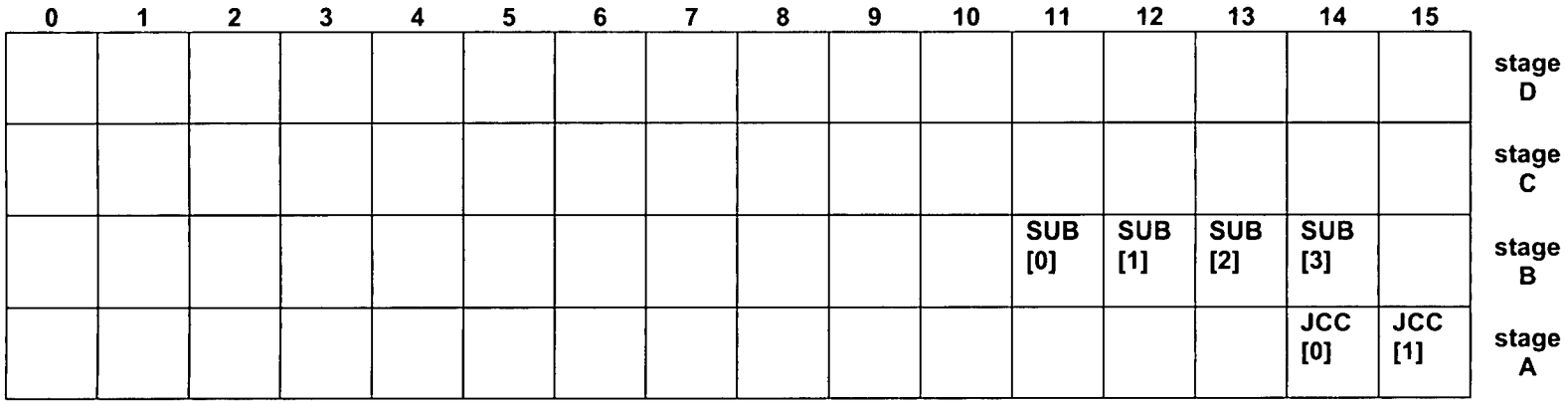
Instruction Buffer Stage Selection Example: Case 4

Figure 4E



current pointer = 14
instruction length = 2
BTAC branch indicator[14] = true
target address[0:3] = 11

next pointer = 0
carry = true
fwrap = false

stage swap mux selects stage B

shift = 1

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Instruction Buffer Stage Selection Example: Case 5

Figure 4F

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
																stage D
											SUB [0]	SUB [1]	SUB [2]	SUB [3]		stage C
JCC [1]																stage B
															JCC [0]	stage A

current pointer = 15
instruction length = 2
BTAC branch indicator[15] = true
target address[0:3] = 11

next pointer = 1
carry = true
fwrap = true

stage swap mux selects stage C

shift = 2

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Instruction Buffer Stage Selection Example: Case 6